REMARKS

The above amendments to the above-captioned application along with the following remarks are being submitted as a full and complete response to the Office Action dated January 18, 2006 (U.S. Patent Office Paper No. 10619463). In view of the above amendments and the following remarks, the Examiner is respectfully requested to give due reconsideration to this application, to indicate the allowability of the claims, and to pass this case to issue.

Status of the Claims

As outlined above, claims 15-23 stand for consideration in this application, wherein claims 1-14 are being canceled without prejudice or disclaimer. In addition, new claims 15-23 are hereby submitted for consideration.

All amendments to the application are fully supported therein. Support for new claims 15-23 may be found on page 16, line 20 - page 18, line 5, Fig. 1,2,4; page 13, lines 8 - 22 and page 18, line 24 - page 19, line 15; page 18, line 16 - page 19, line 23; page 27, line 9 - page 28 line 24; page 27 lines 9 - 24; page 17, lines 2 - 13; page 21, lines 14 - 21; page 7, line 7 - page 8, line 7, Fig. 3; and page 16, line 20 - page 17, line 13, Fig. 4, respectively. Applicants hereby submit that no new matter is being introduced into the application through the submission of this response.

Prior Art Rejections

35 U.S.C. §102(b) rejection

Claims 1-14 were rejected under 35 U.S.C. §102(b) as being anticipated by Miyaoka. As mentioned above, claims 1-14 are being cancelled, and new claims 15-23 are being added. Applicants respectfully traverse this rejection for the reasons set forth below.

According to the M.P.E.P. §2131, a claim is anticipated under 35 U.S.C. §102 (a), (b), and (e) only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference.

Claim 15

The distinctive features of the present invention as now recited in claim 15 is that the clock enable generating circuit invalidates a clock enable signal when a first logical page address requested as a preceding access is the same as a second logical page address

requested as a present access, and a first intra-page address requested as the present access is not within the boundary addresses between intra-page addresses, and the gated logic circuit cuts off the clock to a tag memory when the clock enable signal is valid.

In other words, the gated logic circuit cuts off the clock to the tag memory and the data memory when a second logical page address requested as a present access requested is the same as a first logical page address as a preceding access and a first intra-page address requested as the present access is not within the boundary addresses between intra-page addresses to reduce power consumption. (page 20, line 19 - page 21, line 7 of the specification)

In contrast, Miyaoka merely shows that the CPU ignores the data read from the unit in the buffer storages BSA and BSB if there is no hit between the physical address from the address translation buffer and the physical address from the tag memory, and proceeds with its access to the main storage. (col. 31, line 65 - col., line 12) Miyaoka, however, says nothing about that a gated logic circuit cuts off the clock to the tag memory and the data memory by comparing a present access requested with a preceding access requested.

Therefore, Miyaoka does not show every element recited in claim 15. Accordingly, claim 15 is not anticipated by Miyaoka.

Claims 16-17, 21-23

As to dependent claims 16-17 and 21-23, the arguments set forth above with respect to independent claim 15 are equally applicable here. The base claim being allowable, claims 16-17 and 21-23 must also be allowable.

Claim 18

The distinctive feature as now recited in claim 18 is that a processor executes compressed instructions of VLIW instruction in which a plurality of instruction codes are arranged in a plurality of fields, and the instruction location information decoder outputs control signals to stop the operation clock to the gated clock circuits corresponding to the fields, where the NOP instructions are inserted before the plurality of instruction codes are compressed, on the basis of the instruction location information. When one instruction of the VLIW instructions includes the area where the NOP instruction has been inserted, the operation clock ϕp is no longer supplied to the decode circuits 220 to 223 for decoding such instruction codes and execution circuits 230 to 238 for executing such instruction codes, and

therefore power consumption which has been generated by the decoding and execution of the NOP instruction can be reduced. (Page 29, line 21 – page 30, line 1 of the specification)

In contrast, Miyaoka merely states that a write pulse generation circuit WPG may take on other forms of circuit configuration. Miyaoka, however, does not show any specific structure of WPG. (col. 35, line 67 – col. 36. line 6) In particular, Miyaoka says nothing about a processor executing VLIW instructions in which NOP instructions are inserted.

Therefore, Miyaoka does not show every element recited in claim 18. Accordingly, claim 18 is not anticipated by Miyaoka.

Claim 19

As to dependent claim 19, the arguments set forth above with respect to independent claim 18 are equally applicable here. The base claim being allowable, claims 19 must also be allowable.

Conclusion

In view of all the above, Applicants respectfully submit that certain clear and distinct differences as discussed exist between the present invention as now claimed and the prior art references upon which the rejections in the Office Action rely. These differences are more than sufficient that the present invention as now claimed would not have been anticipated nor rendered obvious given the prior art. Rather, the present invention as a whole is distinguishable, and thereby allowable over the prior art.

Favorable reconsideration of this application as amended is respectfully solicited. Should there be any outstanding issues requiring discussion that would further the prosecution and allowance of the above-captioned application, the Examiner is invited to

contact the Applicant's undersigned representative at the address and telephone number indicated below.

Respectfully submitted,

Stanley P. Fisher
Registration Number 24,344

Juan Carlos A. Marquez
Registration Number 34,072

REED SMITH LLP
3110 Fairview Park Drive
Suite 1400
Falls Church, Virginia 22042
(703) 641-4200

June 19, 2006
SPF/JCM/YM